Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A system on a single integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for decoding the MPEG video data using an external memory to generate video for displaying;

a display engine for processing graphics to be blended with the video using the external memory; and

a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices,

wherein the MPEG video decoder, the display engine and the system bridge controller are implemented on the single integrated circuit chip, [[and]]

wherein ~~the CPU and~~ the plurality of peripheral devices are situated externally to the single integrated circuit chip, and

wherein the external memory has a unified memory architecture, such that the external memory is concurrently used by the CPU through the system bridge controller as at least a

part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

2. (Currently Amended) The system of claim [[1]] 41 wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and one or more of the plurality of peripheral devices.

3. (Previously Presented) The system of claim 2 further comprising other components for processing video and graphics on the single integrated circuit chip, and wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG video decoder and the other components for processing video and graphics.

4. (Canceled)

5. (Currently Amended) The system of claim [[1]] 41 wherein the plurality of peripheral devices include one or more PCI devices, and wherein the system bridge controller includes a PCI bridge for coupling the CPU to the one or more PCI devices.

6. (Original) The system of claim 5 wherein the PCI bridge is capable of performing a DMA function between the one or more PCI devices and an external memory.

7. (Original) The system of claim 5 wherein the PCI bridge is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more PCI devices.

8. (Original) The system of claim 5 wherein the PCI bridge is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more PCI devices.

9. (Currently Amended) The system of claim [[1]] 41 wherein the plurality of peripheral devices include one or more I/O devices, and wherein the system bridge controller includes an I/O bus bridge for coupling the CPU to the one or more I/O devices.

10. (Original) The system of claim 9 wherein the I/O bus bridge is capable of performing a DMA function between the CPU and the one or more I/O devices.

11. (Original) The system of claim 9 wherein the one or more I/O devices include a device selected from a group consisting of ROM, RAM, flash memory and 68000-compatible peripheral devices.

12. (Original) The system of claim 9 wherein the I/O bus bridge is capable of performing format conversion between

big-endian data used in the CPU and little-endian data used in the one or more I/O devices.

13. (Original) The system of claim 9 wherein the I/O bus bridge is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more I/O devices.

14. (Currently Amended) The system of claim [[1]] 41 wherein the system bridge controller includes a CPU interface block for coupling the CPU to the MPEG video decoder.

15. (Original) The system of claim 14 wherein the CPU interface block is coupled with the CPU selected from a group consisting of a MIPS processor, an SH3 processor and an SH4 processor.

16. (Original) The system of claim 14 wherein the CPU interface block is capable of performing burst accesses of the CPU in both read and write directions.

17. (Original) The system of claim 14 wherein the CPU interface block includes one or more buffers used to resolve a speed difference between the CPU and external SDRAM devices.

18. (Previously Presented) The system of claim 14 wherein the CPU interface block is capable of performing format

conversion between big-endian data used in the CPU and little-endian data used in the MPEG video decoder.

19. (Previously Presented) The system of claim 14 wherein the CPU interface block is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the MPEG video decoder.

20. (Currently Amended) The system of claim [[1]] 41 wherein the video includes at least one HDTV video.

21. (Currently Amended) The system of claim [[1]] 41 wherein the video includes at least one SDTV video.

22. (Currently Amended) A method of coupling a CPU to other devices and to process MPEG video data, the method comprising ~~the steps of~~:

coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an integrated circuit chip,

[[wherein]] receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including the MPEG video data; and

~~an MPEG video decoder for~~ decoding the MPEG video data using an MPEG video decoder implemented on the integrated circuit chip to generate video for displaying ~~is implemented on the integrated circuit chip~~,

wherein ~~the CPU and~~ the plurality of peripheral devices are situated externally to the integrated circuit chip.

23. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 22 wherein ~~the step of~~ coupling the CPU to a plurality of peripheral devices comprises ~~the step of~~ performing format conversion between big-endian data and little-endian data, between the CPU and one or more of the plurality of peripheral devices.

24. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 22 wherein the integrated circuit chip contains one or more internal components, and the method further comprises ~~the step of~~ coupling the CPU to at least one of the one or more internal components via the system bridge controller.

25. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 24 wherein ~~the step of~~ coupling the CPU to at least one of the one or more internal components comprises ~~the step of~~ performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the one or more internal components.

26. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 22 wherein ~~the step of~~ coupling the CPU to a plurality of peripheral devices comprises the step of coupling the CPU to one or more PCI devices.

27. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 26 further comprising ~~the step of~~ performing a DMA function between the one or more PCI devices and an external memory.

28. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 26 wherein ~~the step of~~ coupling the CPU to one or more PCI devices comprises ~~the step of~~ performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more PCI devices.

29. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 26 wherein ~~the step of~~ coupling the CPU to one or more PCI devices comprises ~~the step of~~ performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more PCI devices.

30. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 22 wherein ~~the step of~~ coupling the CPU to a plurality of peripheral devices comprises ~~the step of~~ coupling the CPU to one or more I/O devices, the I/O devices being coupled to the integrated circuit chip via a bus different from a PCI bus.

31. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 30 wherein ~~the step of~~ coupling the CPU

to one or more I/O devices comprises ~~the step of~~ performing a DMA function between the CPU and the one or more I/O devices.

32. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 30 wherein the one or more I/O devices include one or more devices selected from a group consisting of ROM, RAM, flash memory and 68000-compatible peripheral devices.

33. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 30 wherein ~~the step of~~ coupling the CPU to one or more I/O devices comprises ~~the step of~~ performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more I/O devices.

34. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 30 wherein ~~the step of~~ coupling the CPU to one or more I/O devices comprises ~~the step of~~ performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more I/O devices.

35. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 24 wherein ~~the step of~~ coupling the CPU to at least one of the one or more internal components comprises ~~the step of~~ performing burst accesses of the CPU in both read and write directions.

36. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 24 wherein ~~the step of~~ coupling the CPU

to at least one of the one or more internal components comprises ~~the step of~~ resolving a speed difference between the CPU and external SDRAM devices.

37. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 24 wherein ~~the step of~~ coupling the CPU to at least one of the one or more internal components comprises ~~the step of~~ performing format conversion between big-endian data used in the CPU and little-endian data used in the MPEG video decoder.

38. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 24 wherein ~~the step of~~ coupling the CPU to at least one of the one or more internal components comprises ~~the step of~~ performing format conversion between little-endian data used in the CPU and big-endian data used in the MPEG video decoder.

39. (Currently Amended) The method of ~~coupling a CPU to other devices of~~ claim 22 wherein the video generated by decoding the MPEG video data includes at least one HDTV video.

40. (Canceled).

41. (Currently Amended) A system on a single integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying; and

a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices, wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip, and

wherein ~~the CPU and~~ the plurality of peripheral devices are situated externally to the single integrated circuit chip.

42-48. (Canceled)

49. (Previously Presented) The system of claim 41, wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor and the MPEG video decoder, and one or more of the plurality of peripheral devices.

50. (Previously Presented) The system of claim 9, wherein the CPU has a first data width that is a multiple of a

second data width of at least one of the one or more I/O devices, and wherein the I/O bus bridge automatically converts a data access with the first data width by the CPU into multiple data accesses with the second data width to support said at least one of the one or more I/O devices having the second data width.

51. (Currently Amended) The method of claim 30, wherein the CPU has a first data width that is a multiple of a second data width of at least one of the one or more I/O devices, and wherein ~~the step of~~ coupling the CPU to one or more I/O devices comprises automatically converting a data access with the first data width by the CPU into multiple data accesses with the second data width to support said at least one of the one or more I/O devices having the second data width.

52. (Cancelled).

53. (Currently Amended) The system of claim [[1]] 41, further comprising a video compositor implemented on the single integrated circuit chip, wherein the video compositor blends the video generated by the MPEG video decoder with graphics.

54. (Previously Presented) The system of claim 53, further comprising a graphics blender implemented on the single integrated circuit chip, wherein the graphics blender blends two or more graphics windows to generate the graphics provided to the video compositor.